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10CS33

Third Semester B.E. Degree Examination, June/July 2015
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Define: i) Rise time ii) Fall time iii) Period and iv) Frequency. **(08 Marks)**

b. What is an universal gate? List the universal gates and prove their universalities. **(06 Marks)**

c. Write the verilog code for the circuit given below. **(06 Marks)**

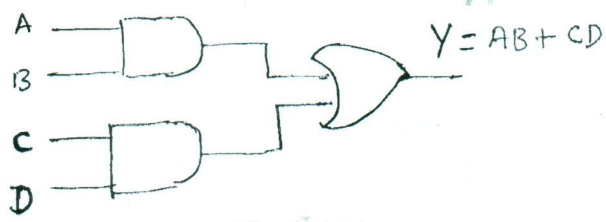

Fig.Q.1(c)

2 a. Using K-map find the reduced SOP form of
$f(A, B, C, D) = \sum M(5, 6, 7, 12, 13) + \sum d(4, 9, 14, 15)$. **(05 Marks)**

b. What is a hazard? List the types of hazards and explain static-0 and static-1 hazards. **(05 Marks)**

c. Simplify the following using Mc-Cluskey method
$F = \sum M (0, 1, 2, 8, 10, 11, 14, 15)$. **(10 Marks)**

3 a. Implement the following function using a 8:1 multiplexer:
$f(a, b, c, d) = \sum M(0, 1, 5, 6, 8, 10, 12, 15)$. **(08 Marks)**

b. Realize the following function using the 3:8 decoder
$F_1(A, B, C) = \sum M (1, 2, 3, 4)$, $F_2(A, B, C) = \sum M (3, 5, 7)$. **(06 Marks)**

c. What is a magnitude comparator? Explain with a neat block diagram an n-bit magnitude comparator. **(06 Marks)**

4 a. With a neat block diagram, explain the working of a Master-Slave JK flip flop. Also write its truth table. **(10 Marks)**

b. Define: i) Flip flop ii) Hold time iii) Set up time iv) Characteristic equation. **(04 Marks)**

c. Calculate the clock cycle time for a system that uses a clock, that has a frequency of
i) 10 MHz ii) 50 MHz iii) 750 kHz. **(06 Marks)**

PART – B

5 a. Draw the logic diagram of a 4-bit serial in serial out shift register using J-K flip flop and explain. **(08 Marks)**

b. Explain briefly serial adder with a neat sketch. **(08 Marks)**

c. Write a verilog code for switched tail counter. **(04 Marks)**

6 a. Briefly explain 3-bit binary ripple up-counter. Also write the truth table and waveform. **(10 Marks)**

b. Design a Modulo-5 up counter (synchronous) using J-k flip flop. **(10 Marks)**

7 a. With neat block diagrams compare Mealy model and Moore model of sequential logic system. **(08 Marks)**

b. Draw the ASM chart for vending machine problem using Mealy model. **(12 Marks)**

8 a. Explain the concept of "Successive approximation" of a A/D converter. **(10 Marks)**

b. Draw a binary ladder network for a digital input 1000 and obtain its equivalent circuit. **(10 Marks)**

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